

	Application No.	Applicant(s)
Notice of Allowability	10/775,025	KIM, JIN-HUN
	Examiner	Art Unit
	Mujtaba K. Chaudry	2112
The MAILING DATE of this communication appeals all claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIOF the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this applied or other appropriate communication IGHTS. This application is subject to	plication. If not included will be mailed in due course. THIS
1. \boxtimes This communication is responsive to <u>8/6/2007</u> .	·	•
2. X The allowed claim(s) is/are 1-23.		
 3. Acknowledgment is made of a claim for foreign priority ur a) All b) Some* c) None of the: 1. Certified copies of the priority documents have 2. Certified copies of the priority documents have 3. Copies of the certified copies of the priority do International Bureau (PCT Rule 17.2(a)). * Certified copies not received: 	e been received. e been received in Application No	
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.	of this communication to file a reply MENT of this application.	complying with the requirements
4. A SUBSTITUTE OATH OR DECLARATION must be subminformal PATENT APPLICATION (PTO-152) which give	nitted. Note the attached EXAMINER es reason(s) why the oath or declara	'S AMENDMENT or NOTICE OF strong is deficient.
 CORRECTED DRAWINGS (as "replacement sheets") must (a) including changes required by the Notice of Draftspers (a) including changes required by the Notice of Draftspers (b) including changes required by the attached Examiner' Paper No./Mail Date Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in the composition of th	son's Patent Drawing Review (PTO- s Amendment / Comment or in the C .84(c)) should be written on the drawing the header according to 37 CFR 1.121(Office action of not the back) of d).
attached Examiner's comment regarding REQUIREMENT	FOR THE DEPOSIT OF BIOLOGIC	AL MATERIAL.
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)	5. ☐ Notice of Informal F 6. ☐ Interview Summary	• •
3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date	Paper No./Mail Da 7. 🔲 Examiner's Amendr	te
Examiner's Comment Regarding Requirement for Deposit of Biological Material	8. ☑ Examiner's Stateme	ent of Reasons for Allowance
92020 g/27/07		

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on June 29, 2007 has been entered and considered. The present application is in condition for allowance.

Reasons for Allowance

Claims 1-23 are allowed. The following is an Examiner's statement of reasons for allowance:

Generally, the present application is related to calculating and writing checksum to a memory. For example, in independent claim 1 of the present application teaches a method of calculating and writing a checksum in a memory comprising: calculating a first checksum by reading a set of first values from the memory and summing the read values and storing the first checksum; calculating a first mode checksum by subtracting a second value written in a predetermined area of the memory from the first check sum; initializing a second checksum to be zero when the first mode checksum does not meet a predetermined condition; calculating a second mode checksum by inverting the second checksum, adding the inverted second checksum to the first mode checksum; and writing the inverted second checksum value in the

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predetermined area of the memory, when the second mode checksum is equal to the second checksum. The foregoing limitations are not found in the prior arts of record. Particularly, none of the prior arts of record teach, in alone or in combination, nor fairly suggest, "...calculating a first checksum by reading a set of first values from the memory and summing the read values and storing the first checksum; calculating a first mode checksum by subtracting a second value written in a predetermined area of the memory from the first check sum; initializing a second checksum to be zero when the first mode checksum does not meet a predetermined condition; calculating a second mode checksum by inverting the second checksum, adding the inverted second checksum to the first mode checksum; and writing the inverted second checksum value in the predetermined area of the memory, when the second mode checksum is equal to the second checksum."

Independent claims 10 and 22 include similar limitations of independent claim 1 and therefore are allowed for similar reasons.

Dependent claims 2-9, 11-21 and 23 depend from allowable independent claims and inherently include limitations therein and therefore are allowed as well.

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Conclusion

Examiner has cited pertinent prior arts in PTO-892 attached. For example, Gentry teaches a circuit and method for generating a checksum for a TCP packet on the fly. A stream of 32-bit data words from a TCP packet is split into two 16-bit data word streams and separately summed using 16-bit adders. The carry-out from the adders is tied to the carry-in thereof so as to incorporate any carry bits generated into the sum. At the end of the data stream, three further summing cycles are used in order to generate the final 16-bit one's complement checksum. First, the two 16-bit data stream partial sums are added together, including any carry bit from one of the adders while the carry-out from the other adder is stored. In the second cycle the stored carry-out and the carry-out from the first cycle are added into the sum. In the third cycle, any carry bit generated in the second cycle is added to the sum so as to produce the final checksum. Kawasaki et al. teach a checksum rewriting device for rewriting a checksum value. This device includes a translating means for, in a case where a packet is inputted having at least one header consists of a plurality of fields including a checksum field is inputted, translating a value of a predetermined field other than the checksum field; a difference value storing means for storing a checksum difference value calculated using a pre-translated value and a translated value of the predetermined field which is translated by the translating means; and a rewriting means for rewriting the value of the checksum field in the header in the packet in which the predetermined field value has been translated by the translating means, to a new value, using the difference value stored in the difference value storing means. Gerbault et al. teach a method of managing integrity defects concerning data written in a rewritable memory of an electronic component, said electronic component being suitable for performing operations that are capable of modifying

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at least some of said data and of interchanging information relating to said operations either offline, directly with a terminal, or else on-line, with an issuer via said terminal. According to the invention, said method consists in: defining firstly "main" data in which an integrity defect is representative of faulty operation of the rewritable memory, and secondly "secondary" data in which an integrity defect is representative either of faulty operation of the rewritable memory, or else of an interruption in the power supply to the electronic component, on each operation, checking the integrity of at least some data; if a check on the integrity of at least some of the main data reveals an integrity defect, preventing any further operation; and if an integrity check on secondary data reveals an integrity defect, allocating at least one default value to at least one item of secondary data, thereby requiring an interchange to be performed on-line during the following operation. The invention is applicable to making secure transactions performed by means of electronic memory cards. Karim et al. teach a method and a computing system compute an incremental checksum corresponding to a data packet. The incremental checksum is computed within one processor cycle of a processor. A first register stores first checksum information corresponding to a data packet. A second register stores second checksum information corresponding to old information being deleted from the data packet. A third register stores third checksum information corresponding to new information being added to the data packet. An incremental checksum circuit, electrically connected to the first register, to the second register, and to the third register, provides resulting checksum information corresponding to the data packet after deleting the old information from the data packet and adding the new information to the data packet. The resulting checksum information is selectively stored in the first register. Slivka et al. teach a mechanism for detecting corruption of computer programs is

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provided. In a preferred embodiment of the present invention, a checksum is used to determine

when a computer program has been corrupted. Upon initially starting a computer program, a

first checksum is calculated for the computer program. When the computer program is requested

to perform an operation, a second checksum is calculated for the computer program. Corruption

of the computer program is indicated when the first checksum does not equal the second

checksum. Additional prior art citations can be found on PTO-892.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817.

The examiner can normally be reached on Mon-Fri 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Jacques Louis-Jacques can be reached on 571-272-6962.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry

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September 27, 2007